Design of Multi-stage Oscillator with Temperature Compensation in 65nm CMOS Process

Jaeho Lee, Wooyoung Choi

Adviser : Prof. Junyoung Song
Outline

Background
Design Target
Circuit Implementation
Verification Results
Conclusions
**Background**

**Application of Oscillator (OSC)**

- Clock generation for any systems

**Requirement of OSC**

- Total 180° phase shift
- Larger number of stage generates slower output frequency
Design Target

Design of Multi-stage OSC

▪ Set maximum frequency (200MHz) with 5-stage
▪ Checking the relationship between number of stage and freq.
  • Design 5, 7, 11 and 21-stage OSC

Reduction of temperature dependency in OSC

▪ Output frequency is decided by the delay of each stage
▪ Variation of temperature affects the delay by changing Vth
▪ Control of P-body can reduce the effect of temp. variation
# Design Specification

<table>
<thead>
<tr>
<th></th>
<th>ROSC 5</th>
<th>ROSC 7</th>
<th>ROSC 11</th>
<th>ROSC 21</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Number of stage</strong></td>
<td>5</td>
<td>7</td>
<td>11</td>
<td>21</td>
</tr>
<tr>
<td><strong>Target Frequency [MHz]</strong></td>
<td>200</td>
<td>142.86</td>
<td>90.91</td>
<td>47.62</td>
</tr>
<tr>
<td><strong>Supply Voltage [V]</strong></td>
<td></td>
<td>1.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Operating Temp. [°C]</strong></td>
<td></td>
<td></td>
<td>0 ~ 100</td>
<td></td>
</tr>
<tr>
<td><strong>Tunable P-body Voltage [V] (V_{DD}=0.8)</strong></td>
<td></td>
<td></td>
<td>0.8 ~ 1.2</td>
<td></td>
</tr>
</tbody>
</table>
Design Methodology

1. Controlling L (Length)
   1. Increasing L ⇒ take more time for charge to go through
   2. Oscillating speed go slower

2. Controlling W (Width)
   1. Increasing W ⇒ much more charge go through
   2. Oscillating speed go faster
Delay Cell (Schematic & Layout)

$L = 0.8\text{um}$
$W = 1\text{um}$
$P/N\text{ ratio} = 2$
Buffer (Schematic & Layout)

$L = 0.06\, \text{um}$

$W = 3.2\, \text{um}$

$P/N \text{ ratio } = 2.65$
Schematic (ROSC5 & Driver)

**ROSC 5 stage**

**Driver**
Layout (ROSC5)

Load buffer

Reset MOS

5 stage ROSC
Layout (Driver)

20.82um

9.195um

Size 1
Size 8
Size 16
Size 32
Size 64
Final layout (TOP)

- Minimize Supply voltage variation

- ROSC 5
- ROSC 7
- ROSC 11
- ROSC 21
- Pad
Post-layout Sim. results (NN, 40°C, 1.2V)

5 stage (192MHz)

7 stage (137MHz)

11 stage (87MHz)

21 stage (46MHz)
# Summary of simulation results

<table>
<thead>
<tr>
<th># of Stage</th>
<th>Target Freq. (Hz)</th>
<th>Pre-layout Sim.</th>
<th>Post-layout Sim.</th>
<th>Diff. (Pre- vs Post-)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>5</td>
<td>200M</td>
<td>175</td>
<td>269.5</td>
<td>149</td>
</tr>
<tr>
<td></td>
<td>Error* (%)</td>
<td>-12.5</td>
<td>34.75</td>
<td>-25.5</td>
</tr>
<tr>
<td>7</td>
<td>142.86M</td>
<td>124.8</td>
<td>192.2</td>
<td>106.5</td>
</tr>
<tr>
<td></td>
<td>Error (%)</td>
<td>-12.4</td>
<td>34.53</td>
<td>-25.45</td>
</tr>
<tr>
<td>11</td>
<td>90.91M</td>
<td>79.44</td>
<td>122.3</td>
<td>67.83</td>
</tr>
<tr>
<td></td>
<td>Error (%)</td>
<td>-12.62</td>
<td>34.53</td>
<td>-25.39</td>
</tr>
<tr>
<td>21</td>
<td>47.62M</td>
<td>41.62</td>
<td>64.09</td>
<td>35.57</td>
</tr>
<tr>
<td></td>
<td>Error (%)</td>
<td>-12.60</td>
<td>34.59</td>
<td>-25.30</td>
</tr>
</tbody>
</table>
Simulation result (Variation of temperature)
Simulation results
(Variation of $V_{DD}$ & P-BODY voltages)

$K_{VCO} = 278.75 \, [\text{MHz/V}]$

$K_{VCO} = -24 \, [\text{MHz/V}]$
Conclusions

Number of gates and frequency are inversely proportional.

Clock speed variation due to temperature can be controlled by...

- $V_{DD} : K_{VCO} = 278.75 \text{ [MHz/V]}$
- P-Body voltage : $K_{VCO} = -24 \text{ [MHz/V]}$
Design Template  
<5,7,11,21stage Ring Oscillator>  

<WooYoung CHOI>
Outline

• Basic concept
• Design Target
• Schematic
• Layout
• Summary
Outline

• **Basic concept**
  • Concept of Ring Oscillator
  • Actual implementation
• Design Target
• Schematic
• Layout
• Simulation result
• Summary
Concept of Ring Oscillator

- Through reset MOS, pulse given to operate ROSC
- Once pulse is given ROSC keep operating
- Odd number of NOT gates are needed to oscillation
- More NOT gate stage make ROSC oscillate slower
Actual implementation (ROSC)

- Add Load buffer to minimize delay difference
- Add Driver to reinforce output signal
Actual implementation (Driver)

- Gate size going bigger by signal go through
  - Signal current increase

- Pros
  - Signal can go through higher capacitance

- Cons
  - Mass current consumption may obstruct oscillation
Outline

• Basic concept

• **Design Target**
  • How to set L / W?

• Schematic

• Layout

• Simulation result

• Summary
Design target

- Observation of oscillator clock speed change with
  - Number of ROSC stage
  - VDD voltage
  - P-BODY voltage
- Target clock speed
  - ROSC 5 stage : 200MHz
  - ROSC 7 stage : 150MHz
  - ROSC 11 stage : 100MHz
  - ROSC 21 stage : 50MHz
- Use Driver to punch through probe Cap(13pF)
How to set L / W?

1. Controlling L
   1. Increasing L => take more time for charge go through
   2. Oscillating speed go slower

2. Controlling W
   1. Increasing W => much more charge go through
   2. Oscillating speed go faster
Outline

• Basic concept
• Design Target
• **Schematic**
  • What is schematic?
  • Schematic (INV_4 & INV_BUF_4)
  • Schematic (ROSC5 & Driver)
  • Simulation result (Pre layout output)
  • What is corner?
• Layout
• Simulation result
• Summary
What is schematic?

Logical implementation
Schematic (INV_4 & INV_BUF_4)

**INV_4**

- \( L = 0.8u \)
- \( W = 1u \)
- \( P/N \) MOS ratio = 2

**INV_BUF_4**

- \( L = 0.06u \)
- \( W = 3.2u \)
- \( P/N \) MOS ratio = 2.65
Schematic (ROSC5 & Driver)

ROSC 5 stage

Driver
### Simulation result (Pre layout output)

<table>
<thead>
<tr>
<th>Test</th>
<th>Output</th>
<th>Spec</th>
<th>Weight</th>
<th>Pass/Fail</th>
<th>Min</th>
<th>Max</th>
<th>FF</th>
<th>FS</th>
<th>NN</th>
<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROSC_5</td>
<td>/OUT_DRIVER</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_5</td>
<td>/OUT_OSC</td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_5</td>
<td>value(freq VT(&quot;/OUT_DRIVE...)</td>
<td>199.7M</td>
<td>243M</td>
<td>243M</td>
<td>224.9M</td>
<td>225.3M</td>
<td>223.1M</td>
<td>199.7M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_7</td>
<td>/OUT_OSC</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>ROSC_7</td>
<td>/OUT_DRIVER</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_7</td>
<td>value(freq VT(&quot;/OUT_DRIVE...)</td>
<td>142.5M</td>
<td>173.3M</td>
<td>173.3M</td>
<td>160.4M</td>
<td>160.8M</td>
<td>159.1M</td>
<td>142.5M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_11</td>
<td>/OUT_OSC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_11</td>
<td>/OUT_DRIVER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_11</td>
<td>value(freq VT(&quot;/OUT_DRIVE...)</td>
<td>90.67M</td>
<td>110.3M</td>
<td>110.3M</td>
<td>102.1M</td>
<td>102.3M</td>
<td>101.3M</td>
<td>90.67M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_21</td>
<td>/OUT_OSC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_21</td>
<td>/OUT_DRIVER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_21</td>
<td>value(freq VT(&quot;/OUT_DRIVE...)</td>
<td>47.51M</td>
<td>57.79M</td>
<td>57.79M</td>
<td>53.49M</td>
<td>53.6M</td>
<td>53.07M</td>
<td>47.51M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_5_TOP_TEST</td>
<td>value(freq VT(&quot;/OUT_DRIVE...)</td>
<td>169.2M</td>
<td>208.1M</td>
<td>208.1M</td>
<td>191.6M</td>
<td>192M</td>
<td>190.2M</td>
<td>169.2M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_5_TOP_TEST</td>
<td>/OUT_DRIVER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_7_TOP_TEST</td>
<td>value(freq VT(&quot;/OUT_DRIVE...)</td>
<td>120.9M</td>
<td>148.7M</td>
<td>148.7M</td>
<td>136.9M</td>
<td>137.2M</td>
<td>135.8M</td>
<td>120.9M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_7_TOP_TEST</td>
<td>/OUT_DRIVER</td>
<td></td>
<td></td>
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<td></td>
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<td></td>
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</tr>
<tr>
<td>ROSC_11_TOP_TEST</td>
<td>value(freq VT(&quot;/OUT_DRIVE...)</td>
<td>77.03M</td>
<td>94.72M</td>
<td>94.72M</td>
<td>87.22M</td>
<td>87.41M</td>
<td>86.56M</td>
<td>77.03M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_11_TOP_TEST</td>
<td>/OUT_DRIVER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_21_TOP_TEST</td>
<td>value(freq VT(&quot;/OUT_DRIVE...)</td>
<td>40.4M</td>
<td>49.68M</td>
<td>49.68M</td>
<td>45.75M</td>
<td>45.85M</td>
<td>45.4M</td>
<td>40.4M</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
What is corner?

Process variations covered by the model.

NMOS doping concentration

PMOS doping concentration
Outline

• Basic concept
• Design Target
• Schematic

• Layout
  • What is layout?
  • Layout (INV_4 & INV_BUF_4)
  • Layout (ROSC5 & Driver)
  • Layout (TOP, Cap work)
  • Simulation result (Post layout output)

• Simulation result
• Summary
What is layout?

Physically implementation
Layout (INV_4 & INV_BUF_4)

INV_4              INV_BUF_4
Layout (ROSC5)

Load buffer

Reset MOS

5 stage ROSC
Layout (Driver)
Simulation result (post layout output)

<table>
<thead>
<tr>
<th>Test</th>
<th>Output</th>
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<th>Max</th>
<th>FF</th>
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<th>SF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROSC_5</td>
<td>/OUT_DRIVER</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_5</td>
<td>/OUT_OSC</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_5</td>
<td>value(freq VT(✓)/OUT_DRIVE...)</td>
<td>199.7M</td>
<td>243M</td>
<td>243M</td>
<td>243M</td>
<td>224.9M</td>
<td>225.3M</td>
<td>223.1M</td>
<td>199.7M</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_7</td>
<td>/OUT_OSC</td>
<td></td>
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<tr>
<td>ROSC_7</td>
<td>/OUT_DRIVER</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_7</td>
<td>value(freq VT(✓)/OUT_DRIVE...)</td>
<td>142.5M</td>
<td>173.3M</td>
<td>173.3M</td>
<td>173.3M</td>
<td>160.4M</td>
<td>160.8M</td>
<td>159.1M</td>
<td>142.5M</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_11</td>
<td>/OUT_OSC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_11</td>
<td>/OUT_DRIVER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_11</td>
<td>value(freq VT(✓)/OUT_DRIVE...)</td>
<td>43M</td>
<td>102.1M</td>
<td>102.3M</td>
<td>102.3M</td>
<td>101.3M</td>
<td>101.3M</td>
<td>100.4M</td>
<td>90.67M</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_21</td>
<td>/OUT_OSC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_21</td>
<td>/OUT_DRIVER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_21</td>
<td>value(freq VT(✓)/OUT_DRIVE...)</td>
<td>53.49M</td>
<td>53.6M</td>
<td>53.6M</td>
<td>53.6M</td>
<td>53.6M</td>
<td>53.6M</td>
<td>47.51M</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_5_TOP_TEST</td>
<td>value(freq VT(✓)/OUT_DRIVE...)</td>
<td>208.1M</td>
<td>191.6M</td>
<td>191.6M</td>
<td>191.6M</td>
<td>190.2M</td>
<td>190.2M</td>
<td>190.2M</td>
<td>169.2M</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_5_TOP_TEST</td>
<td>/OUT_DRIVER</td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_7_TOP_TEST</td>
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<td>134.9M</td>
<td>148.7M</td>
<td>148.7M</td>
<td>148.7M</td>
<td>137.2M</td>
<td>137.2M</td>
<td>137.2M</td>
<td>120.9M</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_7_TOP_TEST</td>
<td>/OUT_DRIVER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_11_TOP_TEST</td>
<td>value(freq VT(✓)/OUT_DRIVE...)</td>
<td>77.03M</td>
<td>94.72M</td>
<td>94.72M</td>
<td>94.72M</td>
<td>87.22M</td>
<td>87.22M</td>
<td>87.22M</td>
<td>77.03M</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_11_TOP_TEST</td>
<td>/OUT_DRIVER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>ROSC_21_TOP_TEST</td>
<td>value(freq VT(✓)/OUT_DRIVE...)</td>
<td>40.4M</td>
<td>49.68M</td>
<td>49.68M</td>
<td>49.68M</td>
<td>45.75M</td>
<td>45.75M</td>
<td>45.85M</td>
<td>45.4M</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROSC_21_TOP_TEST</td>
<td>/OUT_DRIVER</td>
<td></td>
<td></td>
<td></td>
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Why ‘Pre layout’ and ‘Post layout’ is different?
Outline

• Basic concept
• Design Target
• Schematic
• Layout

• Simulation result (Plot)
  • 5 stage ROSC, 7 stage ROSC, 11 stage ROSC, 21 stage ROSC
  • Variation of VDD
  • Variation of P-BODY
  • Variation of Temperature

• Summary
Simulation result (ROSC 5 / ROSC 7)

5 stage ROSC

7 stage ROSC
Simulation result(ROSC11 / ROSC21)

11 stage ROSC

21 stage ROSC
Simulation result (Variation of VDD)

<table>
<thead>
<tr>
<th>VDD</th>
<th>Pre layout</th>
<th>Post layout</th>
<th>Difference</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8</td>
<td>113.8M</td>
<td>93.0M</td>
<td>22.4%</td>
</tr>
<tr>
<td>0.9</td>
<td>142.9M</td>
<td>118.6M</td>
<td>20.5%</td>
</tr>
<tr>
<td>1</td>
<td>171.4M</td>
<td>143.8M</td>
<td>19.2%</td>
</tr>
<tr>
<td>1.1</td>
<td>199.3M</td>
<td>168.4M</td>
<td>18.2%</td>
</tr>
<tr>
<td>1.2</td>
<td>225.3M</td>
<td>192.0M</td>
<td>17.3%</td>
</tr>
</tbody>
</table>

$K_{VCO} = 278.75$ [MHz/V]
Simulation result (Variation of P-BODY)

<table>
<thead>
<tr>
<th>P-BODY</th>
<th>0.8</th>
<th>0.9</th>
<th>1.0</th>
<th>1.1</th>
<th>1.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre layout</td>
<td>123.4M</td>
<td>121.1M</td>
<td>118.6M</td>
<td>116.2M</td>
<td>113.8M</td>
</tr>
<tr>
<td>Post layout</td>
<td>101.7M</td>
<td>99.5M</td>
<td>97.3M</td>
<td>95.1M</td>
<td>93.1M</td>
</tr>
<tr>
<td>Difference</td>
<td>21.3%</td>
<td>21.6%</td>
<td>21.9%</td>
<td>22.2%</td>
<td>22.4%</td>
</tr>
</tbody>
</table>

**RVOSC 5 (Vdd = 0.8)**

- $K_{VCO} = 24$ [MHz/V]

![Graph showing simulation results](image)

- Pre layout
- Post layout
Simulation result (Variation of temperature)

<table>
<thead>
<tr>
<th>Temp</th>
<th>0</th>
<th>10</th>
<th>20</th>
<th>30</th>
<th>40</th>
<th>50</th>
<th>60</th>
<th>70</th>
<th>80</th>
<th>90</th>
<th>100</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre layout</td>
<td>250.1M</td>
<td>243.3M</td>
<td>236.9M</td>
<td>230.9M</td>
<td>225.3M</td>
<td>220.0M</td>
<td>215.3M</td>
<td>210.3M</td>
<td>205.8M</td>
<td>201.6M</td>
<td>197.5M</td>
</tr>
<tr>
<td>Post layout</td>
<td>212.4M</td>
<td>206.8M</td>
<td>201.6M</td>
<td>196.7M</td>
<td>192.2M</td>
<td>187.7M</td>
<td>183.6M</td>
<td>179.7M</td>
<td>176.1M</td>
<td>172.5M</td>
<td>169.2M</td>
</tr>
<tr>
<td>Difference</td>
<td>17.75%</td>
<td>17.65%</td>
<td>17.51%</td>
<td>17.39%</td>
<td>17.34%</td>
<td>17.21%</td>
<td>17.10%</td>
<td>17.03%</td>
<td>16.87%</td>
<td>16.87%</td>
<td>16.73%</td>
</tr>
</tbody>
</table>

**RVOSC 5 (Vdd = 1.2)**
Outline

• Basic concept
• Design Target
• Schematic
• Layout
• Simulation result

• Summary
  • Final layout
  • L & W variation
  • Stage number variation
  • VDD variation
Final layout
Layout (TOP, Cap work)

Minimize Voltage swing
L & W variation
• L increase  => oscillation speed go down
• W increase  => oscillation speed go up

Stage number variation
• Stage number increase => oscillation speed go down

VDD variation
• VDD increase  => Faster oscillation

P-BODY variation
• P-BODY increase  => Slightly slower oscillation